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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/816,492	03/23/2001	Hongyong Zhang	07977-029003 / US3002/326	1777

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EXAMINER
TON, MINH TOAN T

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 05/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/816,492	ZHANG, HONGYONG	
	Examiner	Art Unit	
	Toan Ton	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *08/646,512* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Claim Objections

1. Claim 1 is objected to because of the following informalities: claim 1, line 11, "layer" should be changed –electrode--. Appropriate correction is required.

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-23 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-22 of U.S. Patent No. 6219118. Although the conflicting claims are not identical, they are not patentably distinct from each other because the present applications are broader in scope than the patented claims.

Both set (present and patented) of claims recite the followings:

A display device comprising:

a substrate;

a plurality of parallel source lines and a plurality of parallel gate lines formed over said substrate, said source line and gate lines being arranged relative to one another to form a matrix of pixel regions over said substrate with each of said pixel regions bounded by two adjacent source lines and two adjacent gate lines;

a plurality of thin film transistors formed on said substrate, at least one thin film transistor disposed at each intersection of said source lines and gate lines in each of said pixel regions;

a first interlayer insulating film formed over said thin film transistors;

a black matrix comprising a light shielding electrode formed on said first interlayer insulating film, said light shielding electrode disposed to ("completely," for present claim 1)cover said gate lines;

a second interlayer insulating film formed on said light shielding electrode;

a pixel electrode disposed in each of said pixel regions on said second

interlayer insulating film, wherein a periphery of said pixel electrode overlaps with said light shielding electrode to form an auxiliary capacitor with said light shielding electrode, said second interlayer insulating film and said pixel electrode; and

a counter electrode in electrical communication with said light shielding electrode, wherein said light shielding electrode is electrically connected to a same potential as the counter electrode;

wherein said second interlayer insulating film is interposed between said pixel electrode and said first interlayer insulating film and prevents any direct electrical contact therebetween (see patented claim 2);

wherein said second interlayer insulating film has a flat upper surface over said light shielding electrode (see patented claim 3);

wherein said pixel electrode is transparent (see patented claim 4);

wherein said light shielding electrode comprises chromium (see patented claim 5);

wherein said light shielding electrode comprises titanium (see patented claim 6);

wherein a periphery of said pixel electrode is overlapped with corresponding one of said source lines, and said light shielding conductive layer extends between the pixel electrode and said one of the source lines (see patented claim 7);

wherein said thin film transistors have a top-gate structure (see patented claim 8);

wherein said pixel electrode is overlapped with said light shielding conductive layer with said second insulating layer interposed therebetween to form a capacitor, and a periphery of said

pixel electrode being overlapped with the source lines and the gate lines which define the corresponding pixel region, and said light shielding conductive layer extends between said pixel electrode and said source and gate lines (see patented claim 11);

wherein a periphery of said pixel electrode is overlapped with corresponding ones of gate lines and said light shielding conductive layer extends in an overlapped portion between the pixel electrode and said one of the gate lines (see patented claim 15).

Contact Information

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan Ton whose telephone number is (703) 305-3489. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 0956.

May 5, 2003

TOAN TON
PRIMARY EXAMINER